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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|---------------------|------------------|
| 10/657,193 | 09/09/2003 | Daisuke Ito | 300.1125 | 1637 |
| 21171 | 7590 | 05/19/2005 | EXAMINER | |
| STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005 | | | DANG, TRUNG Q | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2823 | |

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|--------------------------------------|-------------------------------------|--|
| Office Action Summary | Application No. 10/657,193 | Applicant(s) ITO, DAISUKE | |
| | Examiner Trung Dang | Art Unit 2823 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 April 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3, 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US 2004/0166659 of record) in view of Shih et al. (US 6,080,656).

With reference to Figs. 13-15, Lin et al. teach a method of forming a conductor wiring pattern comprising the steps of:

forming a first insulating layer **4** on a surface of a substrate **1**;
forming a photosensitive polymer layer **5** (corresponding to the claimed second photosensitive insulating resin layer) thereon;
light-exposing and developing the photosensitive polymer layer **5** to form pattern grooves **7**, each having sidewalls and a bottom so that the first insulating layer **4** is exposed at the bottom of each pattern groove **7** (Fig. 13 and para. [0059]
forming a plating seed layer **200/202** on the photosensitive polymer layer **5** including inner surfaces of the pattern grooves **7** (Fig. 14);
filling the pattern grooves **7** with copper **210** by an electroplating (same as electrolytic plating) using the plating seed as an electrode (Fig. 15 and

paragraph [0060]; and
chemical mechanical polishing copper layer **210** to form a wiring pattern **212**
consisting of copper remaining in the pattern grooves **7** (Fig. 16).

Lin differs from the claims in that while Lin forms the wiring pattern **212** by blanket electroplating copper to fill the pattern grooves and the performing a CMP process, the claims call for a process to make the same which includes forming a resist pattern on the plating seed layer except for portions of the pattern grooves **7** of the polymer layer **5** so that the seed layer only on sidewalls and bottom of the pattern groove **7** is exposed and then filling the pattern grooves with a conductor by electroplating.

Shih recognizes dishing problem encountered in prior art process of forming conductor wiring pattern, wherein conductor are blanket electroplated to fill pattern grooves followed by a CMP process (Figs. 1-2 and related text). Accordingly, Shih solves the dishing problem by suggesting a method for forming the same which includes the steps of forming a resist pattern 40 on the plating seed layer 20 except for portions of the pattern grooves 30 so that the seed layer 20 only on the sidewalls and bottom of the pattern groove 30 is exposed, filling the pattern grooves 30 with copper 50 by selective electroplating and then removing the resist pattern and the seed layer exposed on the surface of insulating layer 12 (Figs. 4-6 and col. 4, lines 5-37).

It would have been obvious to one of ordinary skill in the art to modify Lin's teaching by forming the wiring pattern **212** according to the aforementioned process suggested by Shih because the selective electroplating would have the benefit over the blanket electroplating process of Lin in that dishing problem is eliminated.

For claims 2 and 3, see para. [0054] in Lin in which a nickel cap layer is used to prevent copper corrosion.

For claim 5, see Fig. 13, wherein metal pad **2** reads on the claimed limitation "electrode terminal".

For claim 6, opening 7' of Fig. 13 corresponds to the claimed "lowest horizontal surface".

For claims 7 and 8, filling the pattern grooves with conductor up to the level as claimed with respect to the thickness of the polymer 5 of the combined process would have been obvious to one skilled in the art because this would ensure no void formation in the deposited conductor layer or dipping on the surface thereof, which could cause breaking or dishing problem during subsequent CMP. Such is within the knowledge of one skilled in the art.

For claim 9, the CMP process of the combined method removes the seeding layer on the horizontal surface of polymer layer 5 but not the seeding layer on the sidewalls and bottom of groove 7 (Fig. 16), that is the seeding layer is selectively removed.

3. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al.

taken with Shih et al. as applied to claims 1-3, 5-9 above, and further in view of Ahmad et al. of record.

The combined process of Lin and Shih teaches a method as described above. The combination differs from the claim in the material used for the first insulating layer **14**.

Ahmad teaches photosensitive polyimide is used as an insulating base on which copper is electroplated to fill openings formed in the insulating base (Figs. 18, 21 and col. 5, lines 64-68).

It would have been obvious to one of ordinary skill in the art to use photosensitive polyimide as material for the first insulating layer **4** of Lin because the use of the photosensitive polyimide material eliminates necessary steps of forming photoresist masks for etching opening **7'** in layers **4** of Fig. 13, hence saving processing step and therefore reducing manufacturing cost. Also, see col. 2, lines 47-49 in Ahmad et al. for the curing of the photosensitive polyimide layer (corresponding to the claimed limitation "the first insulating layer is heated and hardened"). Also, see Fig. 13 in Lin et al., wherein metal wiring **6** reads on the claimed limitations "first wiring pattern formed on the substrate".

Response to Arguments

4. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Trung Dang
Primary Examiner
Art Unit 2823

5/16/05